BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

(An Autonomous institution affiliated to VTU, Belagavi)
Doddaballapur Main Road, Avalahalli, Yelahanka, Bengaluru- 560119



Department of Electronics and Communication Engineering

M. Tech. – VLSI System Design

Scheme (I-IV Semesters)
and
Syllabus (Semester I)

Academic Year: 2025 - 26

Approved by BoS on 09.08.2025

Institute Vision

To emerge as one of the finest technical institutions of higher learning, to develop engineering professionals who are technically competent, ethical and environment friendly for betterment of the society.

Institute Mission

Accomplish stimulating learning environment through high quality academic instruction, innovation and industry-institute interface.

Department Vision

Be a pioneer in providing quality education in electronics, communication, and allied engineering fields to serve as a valuable resource for industry and society

Department Mission

1. To nurture students with a strong foundation in theoretical and practical concepts through innovative pedagogy and industry interface.
2. To foster interdisciplinary research, entrepreneurship skills and instill professional ethics by providing experiential learning opportunities.

Program Educational Objectives (PEOs):

1. Excel in professional career, lead research in the area of VLSI and allied fields.
2. Exhibit professional ethics, effective communication and teamwork in solving engineering problems by adapting industry standards for sustainable development of society.

Program Outcomes (POs):

PO1: An ability to Apply the knowledge of Mathematics, Science and Engineering to solve VLSI Design problems

PO2: An ability to Analyse and design complex VLSI circuits, using suitable analytical methods, Electronic Design Automation (EDA) tools.

PO3: An ability to independently carry out research /investigation and development work to solve practical problems

PO4: An ability to write and present a substantial technical report/document

PO5: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

Scheme (I-IV semester)

M.Tech.- VLSI System Design (VSD)

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

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Scheme of Teaching and Examinations – 2025 Scheme

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2025 – 26 onwards)

I Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD101	ASIC design	EC	3	0	0	3	50	50	100	3	3
2	IPCC	MVSD102	Digital System Design (Lab will be on FPGA)	EC	3	0	1	4	50	50	100	3	5
3	PCC	MVSD103	Digital IC Design	EC	3	0	0	3	50	50	100	3	3
4	PEC	MVSD104X	Professional Elective-I	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD105X	Professional Elective-II	EC	3	0	0	3	50	50	100	3	3
6	PCCL	MVSDL106	Digital IC Design lab	EC	0	0	2	2	50	50	100	3	4
7	NCMC	MRMI107	Research Methodology and IPR	-	-	-	-	-	Online courses (online.vtu.ac.in)				
TOTAL					**15**	**0**	**3**	**18**	**300**	**300**	**600**		

Professional Elective-I		**Professional Elective-II**	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD104A	Static Timing Analysis	MVSD105A	Scripting for VLSI
MVSD104B	On-Chip Communication Architectures	MSVD105B	Advanced Computer Architecture
MVSD104C	RISC-V Architecture and Design	MSVD105C	VLSI Process Technology
MVSD104D	Physics of VLSI Devices	MSVD105D	Micro and Nano devices

Note: PCC: Professional core. **IPCC**- Integrated Professional Core Courses, **PCCL-**Professional Core Course lab, **NCMC**- None Credit Mandatory Course, **L-** Lecture, **P-**Practical, **T/SDA**- Tutorial / Skill Development Activities(Hours are for Interaction between faculty and students), **MRMI107-** Research Methodology and IPR **(Online)** for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

PCC: Professional Core Course: Courses related to the stream of engineering, which will have both CIE and SEE components, students have to qualify in the course for the award of the degree. **Integrated Professional Core Course (IPCC)**: Refers to a Professional Theory Core Course Integrated with practical of the same course. The IPCC's theory part shall be evaluated by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

PCCL: Professional Core Course Laboratory: Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.

Gain confidence in the modeling of systems and algorithms for transient and steady-state operations, thermal study, etc. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s are to be involved either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities that will enhance their skills. The prepared report shall be evaluated for CIE marks.

MRMI107-Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at http://online.vtu.ac.in and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.

MVSD- M.Tech VLSI System Design

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II Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	IPCC	MVSD201	Physical Design	EC	3	0	1	4	50	50	100	3	5
2	PCC	MVSD202	Analog IC Design	EC	4	0	0	4	50	50	100	3	4
3	PCC	MVSD203	VLSI Testing	EC	3	0	0	3	50	50	100	3	3
4	PCC	MVSD204	System Verilog for Verification	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD205X	Professional Elective-III	EC	3	0	0	3	50	50	100	3	3
6	PEC	MVSD206X	Professional Elective-IV	EC	3	0	0	3	50	50	100	3	3
7	PCCL	MVSDL207	Analog IC Design Lab	EC	0	0	1	1	50	50	100	3	3
8	AEC	MVSD208	VLSI Testing and Verification Lab	EC	0	0	1	1	50	50	100	3	2
TOTAL					**19**	**0**	**3**	**22**	**400**	**400**	**800**	-	-

Professional Elective-III		Professional Elective-IV	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD205A	Mixed Signal IC Design	MVSD206A	System on Chip
MVSD205B	RF IC Design	MVSD206B	Low Power VLSI Design
MVSD205C	VLSI Digital Signal Processing	MVSD206C	Bio-Medical CMOS ICs
MVSD205D	High Performance Computing Architectures	MVSD206D	CAD for VLSI

Note: **PCC**: Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab**, PEC-** Professional Elective Courses, **MDC-** Multi-Disciplinary Courses , **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities** (Hours are for Interaction between faculty and students),**L-Lecture, P-Practical, T-Tutorial** (Hours are for Interaction between faculty and students).
Note: **MVSD** means specialization code for example **M.Tech . in VLSI System Design.**

Ability Enhancement Courses (AEC):. These courses are designed to help students enhance their skills in communication, language, and personality development. They also promote a deeper understanding of subjects like social sciences and ethics, culture and human behavior, human rights, and the law.

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III Semester M. Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD301	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
2	PCC	MVSD302	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
3	PCC	MVSD303	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
4	INT	MVSDI304	Internship Phase I (Research/Industry Internship)	EC	0	0	5	5	100	--	100	-	10
5	PW	MVSDP305	Project Phase I	EC	0	0	4	4	100	--	100	-	8
TOTAL					**9**	**0**	**9**	**18**	**200**	**300**	**500**		**18**

- **Professional Core Course (PCC):** It is an Online course and been proctored by the faculty throughout the semester. Students can choose the online course/certification programs from NPTEL (The courses are identified by BOS). They may present the final certificate for internal assessment. Student can take the course during II semester break and need to submit the course completion certificate before semester end examination for evaluation.
- **Internship Phase-I:** All the students shall have to undergo mandatory internship of 4-6 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-I:** Students in consultation with the guide/co-guide if any shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document and present a seminar. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1 shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

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IV Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration(H)	
1	INT	MVSDI401	Internship Phase II (Research/Industry Internship)	EC	0	0	10	10	100	100	200	3	20
2	PW	MVSDP402	Project Phase II	EC	0	0	12	12	100	100	200	3	24
TOTAL					**0**	**0**	**22**	**22**	**200**	**200**	**400**	**-**	**44**

- **Internship Phase-II:** All the students shall have to undergo mandatory internship of 6-8 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-II:** CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. The CIE marks awarded for project work phase -2 shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25. SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check (below 20%).

Syllabus (I semester)

M.Tech.- VLSI System Design (VSD)

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

ASIC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD101**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Learn the ASIC methodologies and programmable logic cells to implement a function on IC.
2. Understand the issues and tools related to ASIC design and implementation
3. Acquire the knowledge of physical design and partitioning methods
4. Summarize the floor planning, placement and routing techniques

Module – 1

Introduction to ASICs:
Types of ASICs: Full Custom ASICs, Standard Cell based ASICs, Gate array based ASICs, Channelled gate array, Channel less gate array, structured gate array, Programmable logic devices, Field Programmable Gate Arrays, Design Flow,
Data logic cells: Data Path Elements, Adders, Multipliers, Arithmetic operator (Practical approach), I/O Cell, Cell Compilers. (8 Hours)

Module – 2

ASIC Library Design:
Logical effort: Predicting delay, logical area and logical efficiency, logical paths, multistage cells, optimum delay, optimum no. of stages. Library cell design.
Programmable ASICS: The Antifuse, Static RAM, EPROM and EEPROM technology (8 Hours)

Module – 3

Programmable ASICs logic cells:
Xilinx LCA: XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis.
Programmable ASIC Design Software: Design System, logic synthesis, Introduction to Synthesis and Simulation.
Low- Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation. (8 Hours)

Module – 4

ASIC Construction:
Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, Power dissipation, FPGA partitioning.
Partitioning methods: partitioning example, Constructive Partitioning, Iterative Partitioning Improvement, Kernighan algorithm, The ratio-cut algorithm, Look Ahead algorithms. (8 Hours)

Module – 5

Floor Planning and Placement & Routing:
Floor planning: Floor planning goals, Floor planning tools, I/O and power planning, clock planning. **Placement:** Placement goals, algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow.
Routing: Global Routing goals and methods, Detail Routing, Left edge algorithm, Area routing algorithm, Special Routing, Circuit Extraction and DRC. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Appreciate the types of ASICs, VLSI design flow and data logic cells.

CO2: Analyze the design parameters for speed, area, power optimization and FPGA programming technologies for design of ASICs

CO3: Apply the features of logic cells, FPGA design flow and design entry required for ASIC design

CO4: Analyze the importance of system partitioning and its methods in the physical design

CO5: Apply the back-end physical design flow, including floor planning, placement and Routing techniques for digital system design.

Suggested Learning Resources:

Text Books:

1. M J S Smith, Application -Specific Integrated circuits, Pearson Education, Seventh impression 2010.

References:

1. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
2. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN:978-14614-4270-7.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview.
2. https://www.scribd.com/document/482509792/ASIC-Lab

M.TECH. VLSI System Design
Choice-Based Credit System (CBCS)
Semester – I

Digital System Design (3:0:1) 4
(Effective from the academic year 2025-26)

Course Code	**MVSD102**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:2	SEE Marks	50
Total Number of Contact Hours	40 Hrs + 10 Lab sessions	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To introduce digital system design using Verilog HDL.
2. To understand synthesis and design optimization for FPGAs.
3. To explore FPGA architectures and programmable logic devices.
4. To design processor subsystems and system-level architectures.

Module – 1

Introduction and Methodology: Digital systems and embedded systems, Binary representation and circuit elements, Real-world circuits, Models, Design methodology

Combinational Basics: Boolean Functions, Boolean Algebra, Verilog Models of Boolean Equations, Using Vectors for Binary Codes, Bit Errors, Decoders and Encoders, Multiplexers, Active-Low Logic (8 Hours)

Module – 2

Number Basics: Unsigned integers, Coding Unsigned Integers, Operations on Unsigned Integers, signed integers, Coding signed Integers, Operations on signed Integers, Fixed and floating-point numbers (8 Hours)

Module – 3

Sequential Basics: Storage elements, Counters, Sequential data paths and control, finite state machines, Clocked synchronous timing methodology (8 Hours)

Module – 4

Memories: Concepts, Memory types, Asynchronous static RAM, Synchronous Static RAM, Dynamic RAM Read-Only Memories, Error detection and correction (8 Hours)

Module – 5

Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description.

Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description.

Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers

Verilog Structural description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (8 Hours)

	PRACTICAL COMPONENT OF IPCC
Sl.NO	**Verilog code design, simulate and synthesize the following with a suitable FPGA**
1	Verilog implementation of 8:1 Mux/Demux.
2	Verilog implementation of 8 to 3 programmable priority Encoder
3	Verilog implementation of Full Adder using structural modeling
4	Verilog implementation of 8-bit ripple carry adder, carry skip adder.

5	Verilog implementation of Flip Flops (D, SR, T, JK)	
6	Verilog implementation of 4-bit shift register (SISO, SIPO, PISO)	
7	Verilog implementation of 4-bit binary up/down/up-down counter with synchronous reset, BCD counter	
8	Sequence generator/detectors, synchronous FSM-Mealy and Moore machine.	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Apply the concepts of number system and digital circuit logic to design digital systems using Verilog.
2. Apply the basics of sequential circuits, including storage elements and finite state machines, to design simple clocked digital systems using Verilog.
3. Analyze the operations of different memory structures and also error detection, correction methods.
4. Design combinational and sequential logic circuits using Verilog constructs at the RTL level.

Suggested Learning Resources:

Text Books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.
2. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream tech press.
3. Bruno, Frank. FPGA Programming for Beginners. Packt Publishing, 2021.

References:

1. Digital Systems Design Using Verilog, 1st Edition, 2015, Charles Roth, Lizy K. John, ByeongKil Lee, Cengage Learning, ISBN-10: 1285051076
2. Digital Design using Verilog, Elsevier, 2007, W. Wolf 5. Stuart S, Simon David & Peter Flake "System Verilog for Design" A guide to using System Verilog for Hardware design and modelling, Springer publication, 2nd Edition, 2006.

Web Resources:

1. https://freevideolectures.com/course/2319/digital-systems-design
2. http://www.asicguru.com/system-verilog/tutorial/introduction/1
3. https://www.chipverify.com/systemverilog/systemverilog-tutorial
4. https://nptel.ac.in/courses/106/108/106108099/
5. https://nptel.ac.in/courses/117/106/117106092/
6. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111 introductory-digital-systems-laboratory-spring-2006/index.htm

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - I

Digital IC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD103**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Lecture Hours	40	Exam Hours	03

Course objectives:

This course will enable students to

1. Learn CMOS process technology Realize digital circuits using different MOS and CMOS techniques
2. Acquire the knowledge of different digital subsystems
3. Analyze different CMOS circuits
4. Design Combinational and sequential Circuits

Module – 1

Basic MOS technology:
Integrated circuits era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Twin tub process, Bi-CMOS technology.

MOS Transistor Theory:
Introduction, MOS Device Design Equations, The Complementary CMOS Inverter- ideal I-V and CV characteristics, Switch level RC delay models. Noise Margin. The Differential Inverter, Transmission Gate (8 Hours)

Module – 2

Performance estimation of static and dynamic CMOS Designs:
CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic, Cascaded Voltage Switch Logic (CV)

Circuit Design Processes:
MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Basic Physical Design of Simple logic gates. (8 Hours)

Module – 3

Delay: Introduction, ,Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths, Input Ordering Delay Effect, Skewed Gates (8 Hours)

Module – 4

Sequential Circuit Design : Sequencing Static circuits, Circuit Design of Latches and flip flops, Conventional CMOS Latches, Conventional CMOS Flip flops, Pulsed Latches, Resettable latches and flip flops. (8 Hours)

Module – 5

Memory Designs and array Structures:
Memory Classification, Memory Architectures and building blocks. The memory core; Read Only Memories (ROM), Non Volatile Read-Write memories, Random Access Memories (RAM). Content Addressable Memories (CAM) Cells designs, Case studies in Memory designs.

(8 Hours)

Course Outcomes: The students will be able to:

- CO1: Apply the CMOS technology concepts in realizing different logical structures
- CO2: Analyse different CMOS circuits
- CO3: Design layouts for different digital structures
- CO4: Design Combinational Circuits and Sequential circuits
- CO5: Evaluate the performance of digital Systems/subsystems using modern tools.

Textbooks

1. N.H. Weste and David Harris**,** "CMOS VLSI Design – A Circuits and Systems Perspective"**,** 2015**,** Fourth Edition , Pearson.
2. Jan M Rabaey, Anatha chandrakasana, Nikolic, Digital integrated circuits, A design Perspective, 2016, second edition, PHI.

References

1. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", John Wiley India Pvt. Ltd, 2008
2. Sung- Mo Kang & Yusuf Leblebici **,** "CMOS Digital Integrated Circuits", Analysis and Design , 3rd Edition, Tata McGrawHill Publishing Company Ltd., New Delhi, 2007.
3. A Hodges, H.G Jackson and R.A Saleh. , Analysis and Design of Digital Integrated Circuits, 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi. 2007.

Web Resources:

1. https://www.youtube.com/playlist?list=PL1w8k37X_6L92ySuv9B0Fg1rMiL1OE1_1
2. https://nptel.ac.in/courses/117106092
3. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

Static Timing Analysis (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104A**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the concepts of delays, timing parameters, and clock behaviour in digital circuits.
2. Explore STA flow resources such as libraries, netlists, parasitics, and constraints for delay estimation.
3. Analyse the impact of noise, crosstalk, and parasitic effects on circuit timing in nanometer designs.
4. Apply STA constraints, recognize timing exceptions, and identify/fix violations such as setup and hold using STA tools.

Module – 1

Introduction: Introduction, timing analysis of digital circuits, Sequential Elements in RTL.
Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay
Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts. (8 Hours)

Module – 2

Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitic, Interconnects, Parasitic Extraction formats, constraints for design, Back annotation. (8 Hours)

Module – 3

Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Cross talk, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design. (8 Hours)

Module – 4

Constraints for STA: Clock Constraints, Other Timing Constraints, External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate (8 Hours)

Module – 5

Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Input / Output Timing Path Checks, DRC Violation Check, Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply timing concepts and delay parameters to analyze combinational and sequential circuits.

CO2: Apply libraries, netlists, and parasitic models in STA flow for delay estimation.

CO3: Analyse the impact of noise and crosstalk on circuit timing and suggest mitigation methods.

CO4: Examine the timing constraints, exceptions and their effect on circuit behaviour.

CO5: Analyse timing violations using STA reports and recommend effective fixes for design closure.

Suggested Learning Resources:

Text Books:

1. Static Timing Analysis for VLSI circuits", R. Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International, 2020.

References:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.

Web Resources:

1. https://nptel.ac.in/courses/106/102/106102181/ NOC: synthesis of digital systems.

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

On-Chip Communication Architectures (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand on chip communication architecture.
2. Explore different standards of on chip communication architecture.
3. Summarize the scocket based and off chip bus interface standards .
4. Explain the models for performance, power and thermal estimation.

Module – 1

Introduction: Trends in System on chip design, ESL design flow, On-chip communication architecture.

Bus based communication architecture: Terminology, characteristics of bus based communication architecture, data transfer modes, bus topology types, physical implementation of bus wires. (8 Hours)

Module – 2

On-Chip communication architecture standards: Amba 2.0, Amba 3.0, IBM core connect, sonics smart interconnect. (8 Hours)

Module – 3

Communication architecture standards : Altera Avalon, Avalon-ST.

Socket-based On-Chip Bus Interface Standards: Open core protocol, OCP Profiles, VSIA Virtual Component Interface**,** Philips Device Transaction Level Protocol, off-chip bus architecture standards. (8 Hours)

Module – 4

Models for Performance Exploration: Static performance estimation models, Dynamic (simulation-based) performance estimation models, hybrid communication architecture performance estimation approaches. (8 Hours)

Module – 5

Introduction To NoC: OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support. (Text 2) (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Summarize architecture, data transfer models and types of bus wires,.
CO2: Apply knowledge of Amba 2.0, 3.0 and standards for interconnection on chip architecture hardware.
CO3: Use socket based and off chip standards for interconnection of components on the chip.
CO4: Analyze the static, dynamic and hybrid system performance models on chip architecture.
CO5: Explore the techniques required for the construction of network on chip.

Suggested Learning Resources:

Text Books:

1. Sudeep Pasricha, Nikil Dutt, " On-Chip Communication Architectures ", Morgan Kaufmann is an imprint of Elsevier.2008
2. SantanuKundu, Santanu Chattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press

References:

1. Frank Bruno,"FPGA Programming for Beginners", Packt Publishing Ltd, 2021
2. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip , Architectures Holistic Design Exploration", Springer

Web Resources:

1. https://nptel.ac.in/courses/106103183
2. https://elearn.nptel.ac.in/shop/partnering-courses/registration-ongoing/advanced-arm-socs-design-batch-3/?v=c86ee0d9d7ed

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

RISC-V Architecture and Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the RISC-V ISA and its design philosophy.
2. Develop assembly-level programming skills using RISC-V.
3. Design and implement RISC-V-based microprocessor cores.
4. Explore privilege levels, interrupts, CSRs, and memory protection.
5. Integrate RISC-V core with SoC components and test on FPGA/simulators.

Module – 1

Introduction to RISC-V Architecture: Evolution of Instruction Set Architectures (ISAs): RISC vs CISC, Introduction to RISC-V: Modular open-source ISA, Base ISA RV32I, RV64I: instruction formats (R, I, S, B, U, J), RISC-V Assembly Language Programming basics, - Register conventions, toolchains, and simulators (Venus, Ripes). (8 Hours)

Module – 2

Instruction Set Extensions and Programming : Arithmetic and logical operations, Load/store and control transfer instructions, RISC-V M-extension (Multiplication/Division), Pseudo-instructions and optimization, Compressed extension (RVC) overview, Assembly programming practices using simulators. (8 Hours)

Module – 3

Microarchitecture and CPU Design: Single-cycle and pipelined processor design, Datapath and control unit architecture, Instruction execution stages: IF, ID, EX, MEM, WB, Hazards: data, control, and structural, Branch prediction and pipelining strategies, RTL implementation overview in Verilog. (8 Hours)

Module – 4

Privilege Architecture, Traps, and CSRs: RISC-V privilege levels: User, Supervisor, Machine, Exception and interrupt handling, Control and Status Registers (CSRs): definitions and access, Physical Memory Protection (PMP), Basic MMU features and address translation, Trap vector configuration and delegation. (8 Hours)

Module – 5

SoC Integration and Open-source Ecosystem: RISC-V-based SoC design: buses (AXI, AHB), peripherals (UART, Timer), Open-source RISC-V cores: PicoRV32, Rocket Chip, VexRiscv, FPGA prototyping of RISC-V SoC, Introduction to LiteX, Freedom Studio, and VexRiscv , Case studies: RISC-V in commercial and academic projects, Emerging extensions: RISC-V Vector, Security, AI (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain the principles and advantages of RISC-V architecture

CO2: Write assembly-level programs using RISC-V instruction sets.

CO3: Design and simulate a RISC-V-based pipelined processor.

CO4: Analyze the role of privilege levels, interrupts, and CSR registers.

CO5: Demonstrate integration of RISC-V cores into SoC platforms using FPGA.

Suggested Learning Resources:

Text Books:

1. David Patterson and Andrew Waterman, The RISC-V Reader: An Open Architecture Atlas, 1st Edition, Strawberry Canyon LLC, 2017.
2. David A. Patterson and John L. Hennessy, Computer Organization and Design RISC-V Edition: The Hardware Software Interface, 2nd Edition, Morgan Kaufmann, 2020.

References:

1. SiFive and RISC-V Foundation Documentation – https://riscv.org/technical/specifications
2. Krste Asanovic et al., The RISC-V Instruction Set Manual: Volume I: User-Level ISA
3. Tutorials and documentation from GitHub repositories for RISC-V cores (e.g., PicoRV32, RocketChip)

Web Resources:

1. https://riscv.org
2. https://github.com/mortbopet/Ripes (RISC-V simulator)
3. https://riscv.org/learn/education/
4. https://riscv.org/technical/specifications/

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Physics of VLSI devices (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Explain basics of semiconductor physics and electronic devices
2. Explain physics and modelling of PN-Junction, MOS Capacitors and MOSFETs
3. Understand and discuss various short channel effects and issues in deep sub-micron MOSFETs
4. Understand physics of multi-gate transistors

Module – 1

Review of fundamentals: Energy bands, Metals, Semiconductors and Insulators, Electrons and Holes

Semiconductors: Direct and Indirect semiconductors, Intrinsic and Extrinsic materials, Density of states, Fermi distribution, Free carrier densities, Boltzmann statistics, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility.

Current flow mechanisms: Drift current, diffusion current, mobility of carriers, current density equation, and continuity equation. (8 Hours)

Module – 2

PN Junctions: Thermal equilibrium physics- Energy band diagrams, space charge layers, Poisson equation, electric fields and potential, p-n Junction under applied bias.

Static current-voltage characteristics, Reverse bias breakdown: Zener breakdown, avalanche breakdown. (8 Hours)

Module – 3

MOS Capacitor: The Ideal MOS capacitor: Accumulation, depletion and strong inversion regions, threshold voltage, Gate work function, Oxide and Interface charges, Body effect, C-V characteristics of MOS at low and high frequency. (8 Hours)

Module – 4

MOSFETs and Compact Models: The MOSFET structure, working principle and drain characteristics, threshold voltage of MOSFET, MOSFET modelling with SPICE Level 1, 2, 3 for above threshold region, subthreshold Characteristics, Effect of gate and drain voltage on carrier mobility in inversion region.

Scaling and Short Channel Effects: Constant electric field and constant power supply scaling, Effect of scaling – Channel length modulation, Punch through, hot carrier degradation, drain induced barrier lowering. (8 Hours)

Module – 5

Modern MOSFET Principles/Quantum Effects and Advanced MOSFET Structures: Classical Mechanics and its drawbacks, Quantum mechanics, 1D problem – particle in a box, electron tunneling., Non-uniform doping in a channel, High-k dielectrics, Deep submicron devices, structure and basic principle of operation: Double & trigate SOIMOSFETs, and FINFETs, Buried Channel MOSFET. (8 Hours)

Course outcomes :

At the end of the course, the student will be able to:

CO1: Understand the band structure and diagrams of semiconductors

CO2: Design the extrinsic semiconductors with specific carrier concentration and model the carrier transport mechanism in semiconductors

CO3: Design of PN – Junction for given specifications

CO4: Understand the physics of MOS capacitors, MOSFETs and spice level models

CO5: Understand short channel effects of MOSFETs and deep submicron devices.

CO6: Understand the basics of multi-gate transistors to mitigate short channel effects.

Suggested Learning Resources:

Text Books:

1. Ben G Streetman and S Banerjee, Solid State Electronic Devices, 7th Edition Pearson 2018
2. Donald A Neamen, Dhrubes Biswas, Semiconductor Physics and Devices, Mc Grew Hill.
3. Nandita Das Gupta and Amitava Das Gupta, Semiconductor Devices: Modelling and Technology, Printice Hall of India,

References:

1. Y P Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, 2011, Third Edition, Oxford University Press, U. S
2. Introduction to Semiconductor Materials and Devices by M. S. Tyagi, John Wiley & Sons, 5th Edition,2005
3. J. P. Colinge and C. A Colinge, Physics of Semiconductor Devices, 2017, Kluwer Academic Publishers U. S.
4. J. P. Colinge, FinFETs and other multi-gate Transistors, 2020, Springer
5. V. Mitin, V. Kochelap, M. Stroscio, Introduction to Nanoelectronics, Cambridge University press, 2008
6. Rainer Waser, Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2003

Web Resources:

1. https://www.youtube.com/watch?v=QQ6Wr5VC3bA

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Scripting for VLSI (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD105A**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Module – 1

LINUX Basics : Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts. (8 Hours)

Module – 2

PERL Basics : History and Concepts of PERL, Scalar Data, Arrays and List Data, Control structures, Hashes, Basics I/O,Regular Expressions, Functions, Miscellaneous control structures, Formats. (8 Hours)

Module – 3

Advanced Topics in PERL: Directory access, File and Directory manipulation, Process management, Packages and Modules -Applications of PERL scripts to Electronic Design Automation. (8 Hours)

Module – 4

TCL basics: An Overview of TCL and Tk, Tcl Language syntax, Variables, Expressions, Lists, Control flow, procedures, Errors and exceptions, String manipulations. (8 Hours)

Module – 5

Python Basics: Introduction to Python, Using Python interpreter, Brief tour on standard library, Control flow Tools, Data structures, Regular Expressions, Classes, Modules, Applications, Python scripts to Electronic Design Automation (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain and apply commands in LINUX environment.
CO2: Develop and execute the Perl scripts.
CO3: Analyze and Handle files, directories and manage processes using Perl scripts.
CO4: Use TCL scripts for automation and Build TCL scripts to Handle files, directories and manage process.
CO5: Develop Python scripts to interpret files and directories.

Suggested Learning Resources:

Text Books:

1. Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 2012, Fourth Edition, Oreilly Publications.
2. John K, Ousterhout, Ken Jones, Tcl and the Tk Toolkit, 2010, Second Edition, Pearson Education, India

References:

1. Guido van Rossum Fred L. Drake, Jr., editor, Python Tutorial Release 3.2.3, 2012, Python Software Foundation.
2. Randal L. Schwartz, Brian D Foy, Tom Phoenix, Learning Perl, 2021, 8th Edition, O'Reilly Media, Inc.
3. Mark Lutz, Learning Python, 2013, 5th Edition, O'Reilly Media, Inc.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc24_ee134/preview
2. https://nptel.ac.in/courses/106106182

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – I

Advanced Computer Architecture (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD105B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

- Understand the concepts of parallel processing and its applications.
- Analyze the performance of different scalar computers.
- Develop pipelining techniques for efficient instruction execution.
- Explore memory hierarchy and cache design for performance optimization.
- Implement hardware for arithmetic operations.
- Discuss instruction set architecture design and its impact on processor efficiency.

Module – 1

Multiprocessors and multi-computers, Multi-vector and SIMD computers, Vector and SIMD Supercomputers, PRAM and VLSI Models, Conditions of Parallelism, Hardware and Software parallelism. (8 Hours)

Module – 2

Advanced processor technology: CISC and RISC Scalar Processor, Memory hierarchy technology, Cache memory organization: Cache Addressing Models, Shared memory organization. (8 Hours)

Module – 3

Linear pipeline processors, Non-linear pipeline processors: Reservation and Latency Analysis, Instruction pipeline design: Instruction Execution Phases, Mechanisms for Instruction Pipelining, Arithmetic design, Superscalar pipeline design. (8 Hours)

Module – 4

Vector Processing principle, Multi-vector multiprocessors, Compound Vector processing, Principles of multithreading, Fine grain multicomputer, Scalable and multithread architectures, Dataflow and hybrid architectures. (8 Hours)

Module – 5

Parallel programming models, Parallel languages and compilers, Parallel programming environments, Synchronization and multiprocessing modes, Message passing program development: Synchronous and Asynchronous Message Passing. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the basic knowledge of partitioning and scheduling in Multiprocessors.

CO2: Analyze cache memory, virtual memory and shared memory organizations.

CO3: Analyze the design properties of Linear and Non - Linear processors.

CO4: Apply the principles of multithreading in hybrid Architectures.

CO5: Write any parallel programming models for various architectures and Applications.

Suggested Learning Resources:

Text Books:

1. K. Hwang, “Advanced Computer Architecture”, Tata McGraw Hill, 3rd Edition, 2018.
2. W. Stallings, “Computer Organization and Architecture”, McMillan, 11th edition, 2022.

References:

1. Hennessy, John L., and David A. Patterson. Computer architecture: a quantitative approach. Elsevier, 2012, 5th Edition.
2. M.J. Quinn, “Designing Efficient Algorithms for Parallel Computer”, McGraw Hill, 1994.

Web Resources:

1. Advanced Computer Architecture: https://onlinecourses.nptel.ac.in/noc23_cs07/preview
2. Advanced Computer Architecture: https://www.cse.iitb.ac.in/~biswa/courses/CS683/main.html

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – I

VLSI Process Technology (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MSVD105C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To understand the principles of semiconductor device fabrication.
2. To study various fabrication processes and technologies used in modern VLSI chip manufacturing.
3. To provide knowledge on photolithography, oxidation, doping, etching, deposition, and metallization.
4. To comprehend the challenges and advances in nanometer process technologies.

Module – 1

Introduction to IC Process Technology : Introduction to IC fabrication and cleanroom concepts, Wafer preparation: Crystal growth, slicing, lapping, polishing, Cleanroom classifications, contamination sources and control, Basic steps in IC fabrication: Overview of CMOS flow, Moore's Law and scaling trends (8 Hours)

Module – 2

Oxidation and Diffusion: Thermal oxidation: Dry and wet oxidation, kinetics, Deal-Grove model, Oxide growth systems and characteristics, Dopant diffusion: Fick's laws, diffusion profiles, Ion implantation: Mechanism, dose, energy, range, Annealing and activation (8 Hours)

Module – 3

Photolithography and Etching: Photolithography: Photoresists (positive & negative), exposure methods, Contact, proximity, and projection printing, Resolution enhancement techniques (RET), Etching: Wet and dry etching, plasma and reactive ion etching (RIE), Etch selectivity, anisotropy, etch rate control (8 Hours)

Module – 4

Thin Film Deposition and Metallization: CVD (Chemical Vapor Deposition): LPCVD, PECVD, APCVD, PVD (Physical Vapor Deposition): Sputtering, evaporation, Dielectric films: SiO_2, Si_3N_4, High-k materials, Metallization: Aluminum, Copper, barrier layers, Electromigration, reliability, and contact formation (8 Hours)

Module – 5

Process Integration and Advanced Technologies: CMOS process integration: Well formation, isolation, gate stack, silicides, LOCOS, STI, LDD, Spacer techniques, Process challenges at sub-10nm nodes, FinFET, SOI, 2.5D, 3D IC process considerations, Reliability and yield analysis. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Analyze different steps in IC fabrication and cleanroom protocols.

CO2: Explain thermal oxidation and diffusion mechanisms in VLSI process flow.

CO3: Illustrate photolithographic patterning and etching techniques.

CO4: Evaluate thin film deposition and metallization processes.

CO5: Discuss advanced process technologies and integration challenges.

Suggested Learning Resources:

Text Books:

1. S.M. Sze and Kwok K. Ng, VLSI Technology, 2nd Edition, McGraw Hill, 2003.
2. S.K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, Wiley, 2nd Edition, 2008.

References:

1. Simon M. Sze, Semiconductor Devices – Physics and Technology, Wiley, 2008.
2. James Plummer, Michael Deal, Peter Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, Pearson, 2nd Edition.
3. Stephen A. Campbell, Fabrication Engineering at the Micro and Nanoscale, Oxford University Press, 2013.

Web Resources:

1. https://nptel.ac.in/courses/117107127
2. https://ocw.mit.edu/courses/6-152j-micro-nano-processing-technology-fall-2005/

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Micro and Nano devices (3:0:0)3
(Effective from the academic year 2025-26)

Course Code	**MSVD105D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the fundamentals of microscale and nanoscale devices used in VLSI systems.
2. Analyze the physics, materials, and scaling limits of semiconductor devices.
3. Explore the design, fabrication, and applications of MEMS and NEMS-based systems.
4. Understand emerging device concepts beyond CMOS and their integration challenges.
5. Learn nano-fabrication techniques and their role in future electronic device technologies.

Module – 1

Introduction to Micro and Nano Devices: Overview of micro/nano device applications in VLSI systems. Semiconductor fundamentals, quantum confinement, density of states, scaling theory. Introduction to MOSFET scaling, short-channel effects. (8 Hours)

Module – 2

MEMS and NEMS Devices: Working principles and structures of MEMS (Micro-Electro-Mechanical Systems) and NEMS (Nano-Electro-Mechanical Systems). Mechanical and electrical transducers: piezoelectric, capacitive, and thermal actuation. (8 Hours)

Module – 3

Nanoelectronic Devices and Materials: Carbon Nanotubes (CNTs), Nanowires, and Quantum Dots. Device physics of CNT-FETs, FinFETs, TFETs, and Spintronic devices. Role of 2D materials (graphene, MoS_2) in nanoelectronics. (8 Hours)

Module – 4

Fabrication Techniques for Micro/Nano Devices: Top-down and bottom-up fabrication. Photolithography, E-beam lithography, Atomic Layer Deposition (ALD), Molecular Beam Epitaxy (MBE), Etching (Dry and Wet). (8 Hours)

Module – 5

Emerging Technologies and Applications: Beyond-CMOS technologies: Tunnel FETs, Negative Capacitance FETs, Memristors, and Neuromorphic Devices. Device-circuit co-design issues. Reliability, variability, and packaging of nano devices. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Understand the principles of micro and nano device physics and scaling behavior
CO2: Analyze the working of MEMS and NEMS devices and integration with VLSI platforms.
CO3: Apply knowledge of nano materials and device concepts for emerging electronic applications.
CO4: Understand the fabrication process flow and challenges in micro/nano manufacturing.
CO5: Evaluate next-generation device technologies and their application in futuristic electronics.

Suggested Learning Resources:

Text Books:

1. Mark Lundstrom, "Fundamentals of Nanotransistors", World Scientific Publishing, 2013.

2. Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture", McGraw-Hill, 2002.

References:

1. George W. Hanson, "Fundamentals of Nanoelectronics", Pearson Education, 2008.
2. Bharat Bhushan (Ed.), "Springer Handbook of Nanotechnology", Springer, 2017.
3. Karl Goser, Jan Dienstuhl, "Nanoelectronics and Nanosystems", Springer, 2004.

Web Resources:

1. NPTEL Course on Nanoelectronics
2. MEMS/NEMS Introduction by MIT

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - I

Digital IC Design LAB (0:0.5:1.5) 2
(Effective from the academic year 2021-22)

Course Code	**MVSDL106**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:1:3	SEE Marks	50
Total Number of Lecture Hours	30	Exam Hours	03

Course objectives:

This course will enable students to

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit, calculate delay, Layout, RC extraction and Post layout simulation of experiments using CMOS Technology.

1. Inverter Characteristics.
2. NAND
3. Full Adder
4. 2:1 Multiplexer
5. D-Flip Flop
6. Synchronous/Asynchronous Counter

Open Ended Experiments

1. SR- Flip Flop
2. Asynchronous Counter
3. Static RAM Cell
4. Dynamic Logic Circuits
5. Linear Feedback Shift Register

BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

(An Autonomous institution affiliated to VTU, Belagavi)
Doddaballapur Main Road, Avalahalli, Yelahanka, Bengaluru- 560119



Department of Electronics and Communication Engineering

M. Tech. – VLSI System Design

Scheme (I-IV Semesters)
and
Syllabus (Semester II)

Academic Year: 2025 - 26

Approved by BoS on 09.03.2026

Institute Vision

To emerge as one of the finest technical institutions of higher learning, to develop engineering professionals who are technically competent, ethical and environment friendly for betterment of the society.

Institute Mission

Accomplish stimulating learning environment through high quality academic instruction, innovation and industry-institute interface.

Department Vision

Be a pioneer in providing quality education in electronics, communication, and allied engineering fields to serve as a valuable resource for industry and society

Department Mission

1. To nurture students with a strong foundation in theoretical and practical concepts through innovative pedagogy and industry interface.
2. To foster interdisciplinary research, entrepreneurship skills and instill professional ethics by providing experiential learning opportunities.

Program Educational Objectives (PEOs):

1. Excel in professional career, lead research in the area of VLSI and allied fields.
2. Exhibit professional ethics, effective communication and teamwork in solving engineering problems by adapting industry standards for sustainable development of society.

Program Outcomes (POs):

PO1: An ability to Apply the knowledge of Mathematics, Science and Engineering to solve VLSI Design problems

PO2: An ability to Analyse and design complex VLSI circuits, using suitable analytical methods, Electronic Design Automation (EDA) tools.

PO3: An ability to independently carry out research /investigation and development work to solve practical problems

PO4: An ability to write and present a substantial technical report/document

PO5: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

Scheme (I-IV semester)

M.Tech.- VLSI System Design (VSD)

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Institution Affiliated to VTU, Belagavi)

Scheme of Teaching and Examinations – 2025 Scheme

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2025 – 26 onwards)

I Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD101	ASIC design	EC	3	0	0	3	50	50	100	3	3
2	IPCC	MVSD102	Digital System Design (Lab will be on FPGA)	EC	3	0	1	4	50	50	100	3	5
3	PCC	MVSD103	Digital IC Design	EC	3	0	0	3	50	50	100	3	3
4	PEC	MVSD104X	Professional Elective-I	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD105X	Professional Elective-II	EC	3	0	0	3	50	50	100	3	3
6	PCCL	MVSDL106	Digital IC Design lab	EC	0	0	2	2	50	50	100	3	4
7	NCMC	MRMI107	Research Methodology and IPR	-	-	-	-	-	Online courses (online.vtu.ac.in)				
TOTAL					**15**	**0**	**3**	**18**	**300**	**300**	**600**		

Professional Elective-I		Professional Elective-II	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD104A	Static Timing Analysis	MVSD105A	Scripting for VLSI
MVSD104B	On-Chip Communication Architectures	MVSD105B	Advanced Computer Architecture
MVSD104C	RISC-V Architecture and Design	MVSD105C	VLSI Process Technology
MVSD104D	Physics of VLSI Devices	MVSD105D	Micro and Nano devices

Note: PCC: Professional core. **IPCC**- Integrated Professional Core Courses, **PCCL-**Professional Core Course lab, **NCMC**- None Credit Mandatory Course, **L-** Lecture, **P-**Practical, **T/SDA**- Tutorial / Skill Development Activities(Hours are for Interaction between faculty and students), **MRMI107-** Research Methodology and IPR **(Online)** for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

PCC: Professional Core Course: Courses related to the stream of engineering, which will have both CIE and SEE components, students have to qualify in the course for the award of the degree. **Integrated Professional Core Course (IPCC)**: Refers to a Professional Theory Core Course Integrated with practical of the same course. The IPCC's theory part shall be evaluated by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

PCCL: Professional Core Course Laboratory: Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.

Gain confidence in the modeling of systems and algorithms for transient and steady-state operations, thermal study, etc. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s are to be involved either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities that will enhance their skills. The prepared report shall be evaluated for CIE marks.

MRMI107-Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at http://online.vtu.ac.in and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.

MVSD- M.Tech VLSI System Design

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Institution Affiliated to VTU, Belagavi)
Scheme of Teaching and Examinations – 2025 Scheme
Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2025 - 26 onwards)

II Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	IPCC	MVSD201	Physical Design	EC	3	0	1	4	50	50	100	3	5
2	PCC	MVSD202	Analog IC Design	EC	4	0	0	4	50	50	100	3	4
3	PCC	MVSD203	VLSI Testing	EC	3	0	0	3	50	50	100	3	3
4	PCC	MVSD204	System Verilog for Verification	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD205X	Professional Elective-III	EC	3	0	0	3	50	50	100	3	3
6	PEC	MVSD206X	Professional Elective-IV	EC	3	0	0	3	50	50	100	3	3
7	PCCL	MVSDL207	Analog IC Design Lab	EC	0	0	1	1	50	50	100	3	3
8	AEC	MVSD208	VLSI Testing and Verification Lab	EC	0	0	1	1	50	50	100	3	2
TOTAL					**19**	**0**	**3**	**22**	**400**	**400**	**800**	-	-

Professional Elective-III		Professional Elective-IV	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD205A	Mixed Signal IC Design	MVSD206A	System on Chip
MVSD205B	RF IC Design	MVSD206B	Low Power VLSI Design
MVSD205C	VLSI Digital Signal Processing	MVSD206C	Bio-Medical CMOS ICs
MVSD205D	High Performance Computing Architectures	MVSD206D	Machine learning hardware Architecture

Note: **PCC**: Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab**, PEC-** Professional Elective Courses, **MDC-** Multi-Disciplinary Courses , **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities** (Hours are for Interaction between faculty and students),**L-Lecture, P-Practical, T-Tutorial** (Hours are for Interaction between faculty and students).
Note: **MVSD** means specialization code for example **M.Tech . in VLSI System Design.**

Ability Enhancement Courses (AEC):. These courses are designed to help students enhance their skills in communication, language, and personality development. They also promote a deeper understanding of subjects like social sciences and ethics, culture and human behavior, human rights, and the law.

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Institution Affiliated to VTU, Belagavi)
Scheme of Teaching and Examinations – 2025 Scheme
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(Effective from the academic year 2025 - 26 onwards)

III Semester M. Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD301	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
2	PCC	MVSD302	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
3	PCC	MVSD303	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
4	INT	MVSDI304	Internship Phase I (Research/Industry Internship)	EC	0	0	5	5	100	--	100	-	10
5	PW	MVSDP305	Project Phase I	EC	0	0	4	4	100	--	100	-	8
TOTAL					**9**	**0**	**9**	**18**	**200**	**300**	**500**		**18**

- **Professional Core Course (PCC):** It is an Online course and been proctored by the faculty throughout the semester. Students can choose the online course/certification programs from NPTEL (The courses are identified by BOS). They may present the final certificate for internal assessment. Student can take the course during II semester break and need to submit the course completion certificate before semester end examination for evaluation.
- **Internship Phase-I:** All the students shall have to undergo mandatory internship of 4-6 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-I:** Students in consultation with the guide/co-guide if any shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document and present a seminar. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1 shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

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IV Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration(H)	
1	INT	MVSDI401	Internship Phase II (Research/Industry Internship)	EC	0	0	10	10	100	100	200	3	20
2	PW	MVSDP402	Project Phase II	EC	0	0	12	12	100	100	200	3	24
TOTAL					**0**	**0**	**22**	**22**	**200**	**200**	**400**	**-**	**44**

- **Internship Phase-II:** All the students shall have to undergo mandatory internship of 6-8 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-II:** CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. The CIE marks awarded for project work phase -2 shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25. SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check (below 20%).

Syllabus (II semester)

M.Tech.- VLSI System Design (VSD)

Approved by BoS on 09.03.2026

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

Physical Design (3:0:1) 4
(Effective from the academic year 2025-26)

Course Code	MVSD201	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:2	SEE Marks	50
Total Number of Contact Hours	40 + 10 Lab Sessions	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Introduce the ASIC physical design flow and partition algorithms of physical design.
2. Explain different floor planning and placement techniques and algorithms.
3. Learn different routing techniques to establish the routing inside and between the blocks.
4. Understand the importance of timing closure parameters required in backend design.

Module – 1

Introduction: Electronic Design Automation (EDA), VLSI Design Flow, VLSI Design Styles, Physical Design Optimizations, Algorithms and Complexity, Graph Theory Terminology, Common EDA Terminology.

Netlist and System Partitioning: Terminology, Optimization Goals, Partitioning Algorithms, A Framework for Multilevel Partitioning, Clustering, Multilevel Partitioning. (8 Hours)

Module – 2

Chip Planning: Introduction to floor planning, Optimization Goals in Floorplanning, Terminology, Floorplan Representations, Floorplan to a Constraint-Graph Pair, Floorplan to a Sequence Pair, Sequence Pair to a Floorplan, Floorplanning Algorithms, Floorplan Sizing, Cluster Growth, Simulated Annealing, Integrated Floorplanning Algorithms, Pin Assignment, Power and Ground Routing, Design of a Power-Ground Distribution Network Planar Routing, Mesh Routing. (8 Hours)

Module – 3

Global and Detailed Placement: Optimization Objectives, Min-Cut Placement, Analytic Placement, Simulated Annealing, Modern Placement Algorithms, Legalization and Detailed Placement.

Clock Tree Synthesis: Need for Clock Distribution, Clock Parameters, Clock Tree Synthesis, Design Constraints, CTS Topologies and PPA, Types of Clock Trees **(Text 2).** Constructing Trees with Zero Global Skew, H tree**,** Clock Tree Buffering in the Presence of Variation **(Text1).**

(8 Hours)

Module – 4

Global Routing: Introduction, Terminology and Definitions, Optimization Goals, Representations of Routing Regions, Rectilinear Routing, Global Routing in a Connectivity Graph, Finding Shortest Paths with Dijkstra's Algorithm.

Detailed Routing: Horizontal and Vertical Constraint Graphs, Left edge algorithm, Introduction to Area Routing, Net Ordering in Area Routing. (8 Hours)

Module – 5

Timing Closure: Introduction, Timing Analysis and Performance Constraints, Static Timing Analysis, Delay Budgeting with the Zero-Slack Algorithm, Net-Based Techniques, Timing-

Driven Routing, Minimization of Source-to-Sink Delay, Gate Sizing, Buffering, Netlist restructuring.

Physical Design Verification: Static Timing Analysis, Design Sign Off, ECO for Design Fix, Physical Design Verification by Formal Methods, Model Checking, Logic Equivalence Checking, LVS, Electromigration, IR and Cross Talk Analysis,DRC,ERC **(Text2).** (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the concepts of VLSI Design Flow**,** graph theory and partitioning algorithms for efficient system partitioning in VLSI physical design.

CO2: Apply the floor planning, pin assignment methods, algorithms for back end design in VLSI flow.

CO3: Apply modern placement algorithms and clock tree synthesis techniques to achieve optimized chip layout with controlled clock skew and power-performance-area.

CO4: Analyze global and detailed routing techniques, algorithms to find shortest path for routing back-end design.

CO5: Apply the concepts of timing closure and design verification methodologies for VLSI physical design

PRACTICAL COMPONENT OF IPCC

Design a digital system using Verilog HDL. Provide the complete structural description blocks. Subsequently, elaborate on the Physical Design steps required to convert this RTL netlist into a GDSII file.

1.	**Logic Synthesis and Constraint Design** **Task:** Synthesize a given design using standard cell libraries. **Key Activities:** Writing SDC (Synopsys Design Constraints). Tabulating standard, sequential, and combinational cell counts. Analyzing timing, area, and power reports to evaluate performance
2.	**Design Import and Floor planning** **Task:** Import the design database into a Physical Design (PD) EDA tool. **Key Activities:** Understanding the New Data Model (NDM) in the flow. Defining the DIE area and CORE area based on specified utilization and shape. Customizing block port placement according to spacing and side constraints
3.	**Macro Placement and Cell Insertion** **Task:** Position macros and internal cells in the floorplan. **Key Activities:** Aligning macros on a specified grid and applying blockages to prevent congestion. Maintaining keep-out margins around macros. Placing endcap and tap cells following rule guidelines.
4.	**Power Planning** **Task:** Establish the power delivery network for the design. **Key Activities:** Creating power stripes and rails. Analyzing connectivity between stripes, rails, standard cells, and macros. Fixing Power-Ground (PG) connectivity and Design Rule Check (DRC) issues.
5.	**Placement and Post-Placement Timing Analysis**

	Task: Place standard cells and optimize the design for performance. **Key Activities:** Optimizing cell placement and identifying routing bottlenecks. Tabulating congestion and cell density. Performing post-placement timing analysis to enhance performance.
6.	**Clock Tree Synthesis (CTS)** Task: Build a clock tree based on specific CTS requirements. **Key Activities:** Building the clock tree and tabulating latency and skew. Performing Post-CTS timing analysis to evaluate timing accuracy
7.	**Detailed Routing and Verification** **Task:** Perform signal routing and ensure design correctness. **Key Activities:** Executing detailed routing and optimizing each step. Performing Design Rule Check (DRC) and Layout v/s Schematic (LVS) verification.
8.	**Post-Route Analysis and Final Sign-off** **Task:** Perform final optimizations and generate files for fabrication. **Key Activities:** Performing post-route timing analysis and optimization. Inserting filler cells and applying dummy metal filling to improve layout density and manufacturing reliability. Generating the final GDSII file for chip fabrication.

Suggested Learning Resources:

Textbooks:

1. Kahng, A.B., Lienig, J., Markov, I.L., Hu, J., "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011.
2. Veena S. Chakravarthi, Shivananda R. Koteshwar, "SoC Physical Design, A comprehensive Guide", Springer, 2022.

References:

1. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Springer, ISBN: 978-0792398398, 2013.
2. M. J. S. Smith, *Application-Specific Integrated Circuits*, Pearson Education, Seventh Impression, 2010.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc26_cs50/preview
2. https://onlinecourses.nptel.ac.in/noc24_ee77/preview
3. https://github.com/The-OpenROAD-Project/OpenROAD
4. https://www.siliconvlsi.com/category/physical-design

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – II

Analog IC Design (4:0:0) 4

(Effective from the academic year 2025-26)

Course Code	MVSD202	CIE Marks	50
Teaching Hours/Week (L: T:P)	4:0:0	SEE Marks	50
Total Number of Contact Hours	50	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Learn the basics of MOS transistor operation, its characteristics, and device models used in analog circuits
2. Analyze of single-stage amplifiers such as common source, common gate, source follower, cascode.
3. Understand frequency response of amplifiers, including the effect of parasitic capacitance and Miller effect.
4. Learn the concepts of differential amplifiers and current mirrors used in analog integrated circuits.
5. Describe concepts of CMOS operational amplifiers, including gain, output swing, slew rate.

Module – 1

Basic MOS Device Physics: MOSFET structure, MOS I/V Characteristics, MOS transconductance, MOS Device Model: MOS device Layout, MOS device capacitance, MOS small signal model, Output resistance. (10 Hours)

Module – 2

Single Stage Amplifier: CS stage with resistance load, CS with diode connected load, Current source load, CS stage with active load, CS with source Degeneration, Source follower, Common-gate stage, Cascode stage. (10 Hours)

Module – 3

Frequency Response of CS stage: General considerations: Miller effect, Association of poles with nodes, Frequency response of common source stage. (10 Hours)

Module – 4

Differential Amplifiers and Current Mirrors: Single ended and differential operation**,** Basic differential pair (qualitative analysis), small signal analysis of basic differential pair, Common mode response, differential pair with MOS loads, Basic current mirror, Cascode current mirror. (10 Hours)

Module – 5

Operational Amplifiers: One-stage opamp : basic topologies, design procedure, Two-stage opamp: Design procedure, frequency response and stability, output swing calculations, slew rate. (10 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply MOS device models and I–V characteristics to determine operating regions and analyze basic MOS transistor behavior in analog circuits.

CO2: Analyze the performance of single-stage amplifiers such as common source, common gate, source follower and cascode configurations.

CO3: Analyze the frequency response of common source amplifiers by determining poles, zeros, and the effect of Miller capacitance.

CO4: Apply differential amplifier and current mirror concepts to analyze gain, common-mode response, and biasing in analog circuits.

CO5: Analyze CMOS operational amplifier architectures and evaluate key performance parameters such as gain, slew rate, PSRR, output swing, and noise.

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Suggested Learning Resources:

Text Books:

1. Behzad Razavi,"Design of Analog CMOS Integrated Circuits",2nd Edition, Tata McGraw-Hill, 2018.

References:

1. Phillip E Allen, Douglas R Holberg,"CMOS Analog Circuit Design", 2nd Edition Oxford University Press,2013.
2. R. Jacob Baker,"CMOS Circuit Design, Layout, Simulation", 2nd Edition, Wiley publications, 2005.

Web Resources:

1. https://elearn.nptel.ac.in/shop/nptel/analog-ic-design/?v=13b5bfe96f3e

M.TECH. VLSI System Design

Choice-Based Credit System (CBCS)

Semester – II

VLSI Testing (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD203**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the VLSI life cycle, importance of testing, and various fault models used in digital circuits.
2. Apply fault simulation techniques to analyse fault behaviour in combinational and sequential circuits.
3. Generate test patterns using ATPG algorithms including D-Algorithm, PODEM, and FAN for combinational and sequential circuits.
4. Design and implement Design for Testability (DFT) techniques including scan design, boundary scan, and BIST.
5. Analyse memory testing strategies and explore formal verification and equivalence checking methods.

Module – 1

Introduction to VLSI Testing and Fault Modelling: VLSI life cycle; Design automation; Importance of Testing; Testing during VLSI life cycle; Faults and errors; Types of Testing. Yield estimation; Test coverage; Brief concepts of Design for Testability (DFT); Brief concepts of Automatic Test Pattern Generation (ATPG). Modelling – Functional, behavioral and structural; Levels of modelling; Brief introduction of simulation and event driven simulation. Fault modelling – Logical fault models; Stuck-at-fault (single and multiple) models; Fault detection; Fault redundancy; Fault equivalence; Fault dominance; Fault sensitization.

(8 Hours)

Module – 2

Fault Simulation: Fault Simulation in combinational and sequential circuits; Serial fault simulation; Parallel fault simulation; Critical path tracing; Fault sampling; Fault analysis. Single stuck-at-fault testing; Fault injection; Fault justification; Fault propagation; D-Algebra (overview). Introduction to bridging faults, delay faults, manufacturing faults, and check-point faults. (8 Hours)

Module – 3

Automatic Test Pattern Generation (ATPG) : ATPG for combinational circuits; D-Algorithm (with worked examples); Outlines of PODEM and FAN algorithms (conceptual overview only). Introduction to sequential logic test. Overview of ATPG tool flows; Test compaction and test grading; Relationship between fault coverage and test quality. (8 Hours)

Module – 4

Design for Testability (DFT): Testability analysis in terms of controllability and observability in combinational and sequential circuits; Probabilistic and simulation-based testability analysis. Ad-Hoc design and testability approaches. Scan cell/register-based testing; Scan design rules and scan design flow; Boundary scan cells. Introduction to test compression

techniques. Introduction to Built-In Self-Test (BIST) – types and testing strategies (Pseudorandom and Pseudo exhaustive testing covered together). Introduction to Fault tolerance. (8 Hours)

Module – 5

Memory Testing and Verification: Semiconductor Memory Organization; Memory Test Patterns; Memory Faults; Memory self-test; Repairable Memories; Error Correcting Codes. Verification by simulation; Co-design and Co-verification. Industry trends and tools in VLSI testing. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Identify and explain VLSI life cycle, importance of testing, fault models, and fault sensitization concepts in digital systems

CO2: Apply serial and parallel fault simulation techniques to analyze fault behavior

CO3: Apply ATPG concepts including D-Algorithm and understand the working principles of PODEM and FAN algorithms

CO4: Design testable circuits using DFT techniques such as scan design, boundary scan, BIST, and test compression.

CO5: Analyze memory fault models, apply memory self-test and error correcting codes, and evaluate formal verification and equivalence checking methods

Suggested Learning Resources:

Textbooks:

1. M. Abramovici, M. Breuer, A. Friedman – Digital Systems Testing and Testable Design, 2014, Jaico Publishing House.
2. M. L. Bushnell, V. D. Agrawal – Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, Springer, 2006.

References Books:

1. A. Miczo – Digital Logic Testing and Simulation, Wiley, 2003.
2. L. Wang, C. Wu, X. Wen – VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann Publishers, 2006.
3. P. K. Lala – Digital Circuit Testing and Testability, Academic Press, 1997.

Web Resources:

1. NPTEL – Digital VLSI Testing (IIT Kharagpur, Prof. Santanu Chattopadhyay) https://nptel.ac.in/courses/117105137
2. NPTEL – VLSI Design Verification and Test (IIT Guwahati, Prof. J. K. Deka) https://nptel.ac.in/courses/106103016

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

System Verilog for Verification (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD204**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:
This course will enable students to:
1. Understand Verification Fundamentals and Testbench Architecture.
2. Develop Procedural Verification Routines.
3. Apply Advanced Randomization Techniques.
4. Implement Concurrency and Inter process Communication.
5. Design and Analyze Functional Coverage Models.

Module – 1

Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered test bench.

Data Types: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, packages, Streaming Operators, Enumerated types, constants and strings, Expression width. (8 Hours)

Module – 2

Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values.

Connecting the Test bench and Design: Separating the test bench and design, the interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions. (8 Hours)

Module – 3

Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, Inline constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control, Random Number Generators. (8 Hours)

Module – 4

Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, analyzing coverage data, measuring coverage statistics during simulation. (8 Hours)

Module – 5

Universal Verification Methodology (UVM): UVM Overview, UVM Testbench and Environments, interface UVCs, System and Module UVCs, The Verilog UVM class library.

UVM Library Basics: UVM library, Library Base classes, UVM object class, UVM component

class, UVM configuration mechanism, Transaction Level Modelling in UVM, Key TLM concepts in UVM, UVM factory, UVM message facilities, Creating the sequencer. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- CO1: Illustrate procedural statements, tasks, and functions to develop verification routines in System Verilog
- CO2: Illustrate procedural statements, tasks, and functions to develop verification routines in System Verilog
- CO3: Apply constrained random stimulus generation techniques to create randomized verification environments
- CO4: Choose System Verilog concurrency and inter-process communication mechanisms to control and synchronize verification processes
- CO5: Develop functional coverage models and apply UVM concepts to build reusable verification components and environments

Suggested Learning Resources:

Text Books:

1. Chris Spear, "System Verilog for Verification", Springer Publication, 3rd edition, 2012.
2. Sharon Rosenberg and Kathleen A. Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Cadence Design Systems, USA, 2010.

References:

1. Simon Davidmann, "System Verilog for Design", Peter Flake Springer Publications Second Edition, 2006.
2. Bergeron, Janick, "Writing testbenches using System Verilog ", Springer Science & Business Media, 1st Edition, 2007.

Web Resources:

1. VLSI Verify – System Verilog & UVM Tutorials: https://vlsiverify.com/systemverilog/
2. Universal Verification Methodology (UVM) Tutorial https://learn.verificationstudio.com/tutorials/2/universal-verification-methodology-uvm-tutorial

M.Tech in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - II

Mixed Signal IC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	MVSD205A	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Lecture Hours	40	Exam Hours	03

Course objectives:

This course is aimed to

1. Introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Analyze various CMOS circuits Sample and Hold, ADCs, DACs, PLL
3. Design and Implementation ADC & DAC circuits

Module – 1

Review of two stage OP amp: Fundamentals OP-amp based circuits, different features of op-amp(ideal and practical), Parasitic effects on design of 2 stage OP amp, wide swing cascade current mirrors, design of rugged biasing circuit with temperature independent compensation, Challenges in mixed signal circuit design. (Text-1, chapter-6).

Sample-and-Hold Circuits: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection.((Text-1, chapter-11). (10 Hours)

Module – 2

Switched Capacitor Circuits:

Introduction to Switched Capacitor Circuits: Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor (Text-1, chapter-14)

Data Converter Fundamentals: Offset and gain Error - Linearity errors(DNL and INL) - Dynamic Characteristics – SNR, THD and SNDR - Quantization noise spectrum (Text-1, chap-16,17, Text-3, 28,29,20). (8 Hours)

Module – 3

Analog to Digital Converters (ADCs :) Architectures: Flash ADC, Pipeline ADC and SAR ADC (Text-1, chap-17,18, Text-3, 28,29,20). (7 Hours)

Module – 4

Digital to Analog Converters (DACs): Architectures: R2R DAC, Current steering DAC and Charge Scaling DAC (Text-1, chap-16,17, Text-3, 28,29,20). (7 Hours)

Module – 5

PLL: Simple PLL: Phase detector, PLL topology, Dynamis of PLL, Charge pump PLLs: Problem of lock acquisition, phase /frequency detector and charge pump, basics of charge pump.

Design Case studies on PLL(Text-1, chap-19 , Text-2, Chap-16). (8Hours)

Course Outcomes:

The students will be able to:

CO1: Apply the fundamentals of Linear ICs in Mixed signal circuits /designs

CO2: Analyze CMOS based Switched Capacitor Circuits and Sample and Hold circuits

CO3: Design Sample and Hold Circuits using MOS by considering the non idealities.

CO4: Analyze the architectures of ADCs ,DACs and PLL

CO5: Evaluate the performance of Mixed signal ICs for different applications

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits" McGraw Hill Education, 2017, 2nd Edition.
3. R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, 3rd Edition (for Data converter 28th, 29th and 30th Chapters)

References:

1. Ahmed Ali, High Speed Data Converters, 2016, 1st Edition, IET Materials, Circuits& Devices
2. Rui Paulo da Silva Martins and Pui-In Mak, "Analog and Mixed-Signal Circuits in Nanoscale CMOS", Springer, 2024.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – II

RF IC Design (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD205B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the concepts of time variance and noise effects in RF circuits
2. Acquire the knowledge receiver and transmitter architecture at RF frequency
3. Know the role of matching networks, performance parameters and LNA
4. Summarize the mixers, oscillators and phase locked loops

Module – 1

Units in RF design:

Nonlinearity and Time Variance: Effects of nonlinearity -harmonics, gain compression, desensitization, cross modulation, intermodulation, cascaded nonlinear stages.

Noise in RF circuits-Representation of noise in circuits, Input referred noise, Noise figure, Noise figure of cascaded stages, Noise figure of lossy circuits, Sensitivity and Dynamic range, Passive impedance transformation. (8 Hours)

Module – 2

Transceiver architectures:

Receiver Architectures: Heterodyne – constant LO and constant IF down conversion, problem of image, image rejection vs channel selection, dual IF topology, Homodyne – simple homodyne and homodyne with quadrature down conversion, issues in homodyne receivers, Image Reject – Hartley & Weaver architecture. Transmitter architectures - Direct conversion and two-step transmitters. Review of two port parameters and their significance. Nano scale MOSFETs - Parasitic resistances (Rs, Rd, Rg), parasitic capacitances (Cgs, Cgd,), simplified and extrinsic small-signal models. High-frequency figures of merit: f_t and $f_{max.}$ (8 Hours)

Module – 3

Matching networks: Passive RLC circuits, impedance transformation – Quality factor, series to parallel conversion, basic matching networks- L, Pi-match networks – design example. Low noise Amplifier - Performance parameters, Problem of Input matching, CS stage with inductive load, Cascode CS stage with inductive degeneration (MOSFET circuits only), Noise figure calculation, Amplifier bandwidth extension techniques, Millimetre Wave LNAs. (8 Hours)

Module – 4

Mixer: Performance parameters, Mixer noise figures, single balanced and double balanced (active and passive) – working (MOSFET circuits only), Millimeter Wave Mixers. Oscillators - Performance parameters, Feedback view and one port view of oscillators, Cross coupled oscillator, three-point oscillators, (MOSFET circuits only), Ring oscillators. (8 Hours)

Module – 5

Phase Locked Loops: Basic concepts - Phase detector, Type I PLL, Dynamics of simple PLL, Drawbacks of simple PLL, Type II PLLs - PFD, charge pump, charge pump PLL, PFD/CP Non idealities (concepts only) – Up and Down Skew and Width Mismatch, Charge Injection and clock

feed through. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Understand the effects of nonlinearity and noise in RF circuits

CO2: Apply the concepts of homodyne, heterodyne, quadrature for analysing the RF transceivers.

CO3: Appreciate the need for LNA and learn different LNA topologies and design techniques.

CO4: Analyze the various types of synthesizers, oscillators and their characteristics

CO5: Analyze dynamics of PLL and types of PLL with charge injection, clock feed through

Suggested Learning Resources:

Textbooks:

1. Behzad Razavi, *RF microelectronics*. Vol. 2. New York: Prentice hall, 2012.

References:

1. Thomas H Lee, "The Design of CMOS Radio Frequency Integrated Circuits",2nd Edition, Cambridge
2. University Press, 2004, ISBN: 9780511817281 S. Voinigescu, "High-Frequency Integrated Circuits", The Cambridge RF and Microwave Engineering Series, 1st edition, 2013, ISBN: 978-0521873024
3. John Rogers, CalvinPlett, "Radio Frequency Integrated Circuits Design", Artech House, 2003, ISBN: 1-58053-502-x

Web Resources:

1. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering, IIT Kharagpur

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

VLSI Digital Signal Processing (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD205C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the fundamentals of digital signal processing algorithms and their VLSI implementation.
2. Analyze architectural transformations for high-speed and low-power DSP systems.
3. Apply pipelining, parallel processing and retiming techniques in DSP architecture.
4. Design efficient VLSI architectures for DSP algorithms such as filters and transformers.
5. Evaluate performance optimization techniques in VLSI DSP systems.

Module – 1

Introduction to VLSI DSP Systems

Overview of digital signal processing systems, DSP algorithms and applications, challenges in VLSI implementation of DSP systems, design metrics for DSP architectures, introduction to data flow graphs, basic DSP architectures. (8 Hours)

Module – 2

Pipelining and Parallel Processing

Pipelining in DSP systems, pipelining techniques in digital filters, parallel processing in DSP architectures, throughput improvement techniques, unfolding transformation, systolic array architectures. (8 Hours)

Module – 3

Retiming and Architectural Transformations

Retiming techniques, retiming algorithms, folding transformation, register minimization techniques, loop unrolling, scheduling and resource allocation in DSP architectures. (8 Hours)

Module – 4

VLSI Architectures for DSP Algorithms

Architectures for FIR filters, IIR filters, multiplier architectures, FFT architectures, systolic array implementation of DSP algorithms, hardware optimization techniques. (8 Hours)

Module – 5

Low Power and High-Performance DSP Architectures

Low power design techniques for DSP systems, power optimization in DSP architectures, memory and interconnect considerations, implementation using FPGA/ASIC platforms, emerging trends in VLSI DSP design. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain DSP algorithms and their VLSI implementation challenges.

CO2: Apply pipelining and parallel processing techniques to improve DSP system performance

CO3: Analyze retiming and architectural transformation techniques in DSP architectures.

CO4: Design efficient VLSI architectures for digital filters and transform algorithms.

CO5: Evaluate low power and high-performance design techniques in VLSI DSP systems.
Suggested Learning Resources: **Textbooks:** 1. Keshab K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley & Sons, 1999. 2. Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, Springer, 4th Edition, 2014. **References:** 1. Sanjit K. Mitra, Digital Signal Processing: A Computer-Based Approach, McGraw-Hill Education, 4th Edition, 2011. 2. Behrooz Parhami, Computer Arithmetic: Algorithms and Hardware Designs, Oxford University Press, 2nd Edition, 2010. **Web Resources:** 1. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering, IIT Kharagpur

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

High Performance Computing Architecture (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD205D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives

This course will enable students to:

1. Understand the architectural principles and performance metrics of high-performance computing systems.
2. Analyze parallel processor architectures including multicore, manycore, and accelerator-based systems.
3. Evaluate memory hierarchy and interconnection networks used in scalable computing systems.
4. Apply parallel programming models and performance optimization techniques.
5. Examine modern HPC architectures including GPU computing and heterogeneous systems.

Module – 1

Fundamentals of High-Performance Computing:
Introduction to high performance computing, need for HPC systems, parallel computing concepts, Flynn's taxonomy, performance metrics and benchmarks, speedup, efficiency and scalability, Amdahl's law and Gustafson's law, roofline performance model, overview of modern HPC systems. (8 Hours)

Module – 2

Parallel Processor Architectures:
Instruction level parallelism, pipelining and superscalar processors, vector processors and SIMD architectures, multicore and manycore architectures, simultaneous multithreading, GPU architecture basics, heterogeneous computing systems, accelerator-based architectures. (8 Hours)

Module – 3

Memory Hierarchy and Cache Coherence:
Memory hierarchy design, cache organization and optimization, cache coherence protocols (snooping and directory based), shared memory multiprocessors, distributed memory systems, NUMA architectures, memory consistency models, memory performance optimization. (8 Hours)

Module – 4

Interconnection Networks for HPC:
Interconnection network fundamentals, network topology design, bus-based and crossbar systems, multistage interconnection networks, mesh, torus and hypercube topologies, routing algorithms, network latency and throughput, congestion control techniques. (8 Hours)

Module – 5

Parallel Programming Models and HPC Systems:
Parallel programming paradigms, shared memory programming with OpenMP, distributed memory programming with MPI, GPU programming using CUDA/OpenCL, synchronization mechanisms, load balancing techniques, performance optimization and energy-efficient HPC architectures.

(8 Hours)

At the end of the course, the student will be able to:

CO1: Explain the architectural concepts and performance metrics of high-performance computing systems.

CO2: Analyze parallel processor architectures including multicore, many core and accelerator-based systems.

CO3: Evaluate memory hierarchy and cache coherence mechanisms in multiprocessor systems.

CO4: Analyze interconnection network architectures used in scalable HPC systems.

CO5**:** Apply parallel programming models and performance optimization techniques for high performance computing applications.

Suggested Learning Resources:

Textbooks

1. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability and Programmability, McGraw Hill.
2. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann.

Reference Books

1. Michael J. Quinn, Parallel Programming in C with MPI and OpenMP, McGraw Hill.
2. David B. Kirk and Wen-mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, Morgan Kaufmann.
3. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture, McGraw Hill.

Web Resources

1. **NPTEL – High Performance Computing**
   https://nptel.ac.in/courses/106106183
2. **CUDA Programming Guide – NVIDIA**
   https://developer.nvidia.com/cuda-zone
3. **MPI Tutorial**
   https://mpitutorial.com
4. **OpenMP Official Documentation**
   https://www.openmp.org

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – II

System on Chip (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD206A**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores
2. Understand the needs high-level language (in this case, C) in application development
3. Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
4. learn different ARM integer cores, concept of memory hierarchy and management.

Module – 1

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI)

(8 Hours)

Module – 2

The ARM Instruction Set (Continued) Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture (8 Hours)

Module – 3

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements ,Loops, Functions and procedures, Use of memory, Run-time environment.

(8 Hours)

Module – 4

Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support)

(8 Hours)

Module – 5

ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises. Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

(8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- CO1: Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
- CO2: Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
- CO3: Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
- CO4: Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.
- CO5: Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Suggested Learning Resources:

Textbooks:

1. Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2ndedition
2. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2nd edition,
3. 2010.

References Books:

1. Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
2. Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

Web Resources:

1. ARM SoC Design Guide – **https://developer.arm.com/documentation**
2. EDA Playground (for practice with SoC-related Verilog/SystemVerilog simulations): **https://www.edaplayground.com**

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – II

Low Power VLSI Design (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD206B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the concepts of VLSI circuits for low power consumption
2. Acquiring the knowledge of voltage scaling techniques for low power consumption
3. Know the role of capacitance and leakage power in power consumption
4. Summarize the charging techniques, battery design techniques for low power VLSI

Module – 1

Sources of Power dissipation:

Dynamic Power Dissipation -Short Circuit Power, Switching Power, Glitching Power, Leakage Power Dissipation. (8Hours)

Module – 2

Supply Voltage Scaling Approaches:

Device Feature Size Scaling, Architectural level approaches, Voltage scaling using high-level transformations, Multilevel Voltage Scaling, Dynamic Voltage and Frequency Scaling, , Adaptive Voltage Scaling, Sub threshold logic Circuits. (8Hours)

Module – 3

Switched Capacitance Minimization Approaches:

Hardware Software Trade off, Bus Encoding, Clock Gating, Gated-Clock FSMs, FSM State Encoding, Logic Styles for Low Power. (8Hours)

Module – 4

Leakage Power minimization Approaches:

Variable-threshold-voltage CMOS (VTCMOS) approach, Transistor stacking, multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Power management, Dual-Vt assignment approach (DTCMOS), Dynamic V_{th} Scaling. (8Hours)

Module – 5

Adiabatic Logic Circuits:

Introduction, Adiabatic Charging, Adiabatic Amplification, Adiabatic Logic Gates, Pulsed Power Supply, Stepwise Charging Circuits.

Power Estimation: Modeling of signals, Signal probability calculation, Probabilistic Techniques for signal activity, statistical Techniques. (8Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the knowledge of physics of semiconductor to find various sources of power dissipation at the device level.

CO2: Apply different voltage scaling techniques to minimize power dissipation during the design at different levels of abstraction.

CO3: Describe the hardware & software methods of minimizing switched capacitance, leading to low power dissipation.

CO4: Apply multiple threshold voltage, variable threshold voltage, power management methods to minimize the leakage power dissipation.

CO5:	Describe adiabatic concepts, battery power management techniques to improve the power performance of VLSI circuit.

Suggested Learning Resources:

Text Books:

1. Pal, Ajit, Low-Power VLSI Circuits and Systems, Springer publisher, 2015
2. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter-science, 2000

References:

1. K.S. Yeo and K. Roy, Low-Voltage Low-Power Subsystems, McGraw Hill, 2004.
2. J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems", Springer, 2009

Web Resources:

1.NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur.

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

Biomedical CMOS IC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD206C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:
This course will enable students to:

1. Understand the fundamentals of biomedical signal acquisition and processing using CMOS circuits.
2. Analyze low-power and low-noise analog circuit techniques for biomedical applications.
3. Design CMOS circuits for bio signal amplification and filtering.
4. Evaluate implantable and wearable biomedical integrated circuits.
5. Examine energy-efficient architectures for biomedical sensing systems.

Module – 1

Introduction to Biomedical IC Systems
Overview of biomedical instrumentation, bio signal characteristics (ECG, EEG, EMG), requirements of biomedical ICs, noise sources in biomedical circuits, challenges in implantable and wearable devices, introduction to CMOS technology for biomedical applications. (8 Hours)

Module – 2

Low Noise Amplifiers for Biomedical Signals
Low-noise amplifier (LNA) design principles, instrumentation amplifiers, chopper stabilization techniques, noise analysis in CMOS circuits, offset reduction methods, design considerations for ultra-low power amplifiers. (8 Hours)

Module – 3

Analog Front-End Circuits for Bio signal Acquisition
Analog front-end architecture, signal amplification and filtering, band-pass filters for biomedical signals, ADC interfaces, artifact removal techniques, low-power circuit design for bio signal processing. (8 Hours)

Module – 4

Implantable and Wearable Biomedical ICs
Design considerations for implantable ICs, wireless power transfer, biomedical telemetry systems, low-power communication circuits, safety and reliability considerations in biomedical implants. (8 Hours)

Module – 5

Advanced Biomedical CMOS Architectures
Energy-efficient biomedical IC design, neural recording systems, biosensor interfaces, system-on-chip solutions for biomedical applications, emerging trends in biomedical integrated circuits. (8 Hours)

Course Outcomes (Course Skill Set)
At the end of the course, the student will be able to:

CO1: Explain the characteristics of biomedical signals and requirements of biomedical IC systems.
CO2: Analyze low-noise amplifier circuits used for biomedical signal acquisition.
CO3: Design analog front-end circuits for bio signal amplification and filtering.
CO4: Evaluate implantable and wearable biomedical IC architectures.
CO5: Analyze energy-efficient CMOS architecture for biomedical sensing systems.

Suggested Learning Resources:

Textbooks

1. R. Sarveshwar, Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications and Bio-Inspired Systems, Cambridge University Press.
2. Sandro Carrara, Introduction to Biomedical Circuits and Systems, Springer.

Reference Books

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits" McGraw Hill Education, 2017, 2nd Edition.

Web Resources

1. **NPTEL – Biomedical Signal Processing and Instrumentation**
   https://nptel.ac.in
2. **IEEE Biomedical Circuits and Systems Society**
   https://ieee-bio.org

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

Machine Learning Hardware Architectures (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD206D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the fundamentals of machine learning algorithms and their computational requirements.
2. Analyze hardware architectures used for accelerating machine learning workloads.
3. Evaluate parallel computing techniques used in ML accelerators such as GPUs and TPUs.
4. Apply VLSI design concepts for implementing efficient ML hardware architectures.
5. Examine energy-efficient and high-performance architectures for deep learning system

Module – 1

Introduction to Machine Learning Hardware: Overview of machine learning and deep learning, computational characteristics of ML workloads, matrix and tensor operations, challenges in ML hardware implementation, hardware–software co-design, overview of ML accelerators and edge AI hardware. (8 Hours)

Module – 2

Neural Network Architectures and Computation: Artificial neural networks, convolutional neural networks (CNNs), recurrent neural networks (RNNs), deep neural networks (DNNs), computation patterns in neural networks, matrix multiplication and convolution operations, dataflow models for neural networks. (8 Hours)

Module – 3

Hardware Acceleration for Machine Learning: GPU architecture for ML workloads, tensor processing units (TPUs), FPGA-based ML accelerators, systolic array architectures, parallel processing techniques, hardware optimization for neural network computations. (8 Hours)

Module – 4

Memory and Dataflow Architectures: Memory hierarchy for ML accelerators, data reuse techniques, on-chip buffers and scratchpad memories, bandwidth and latency issues, dataflow architectures for neural network acceleration, communication and interconnect challenges. (8 Hours)

Module – 5

Energy Efficient ML Hardware and Edge AI: Energy-efficient ML architectures, model compression techniques (quantization and pruning), hardware support for low precision computation, edge AI accelerators, hardware-software co-optimization, emerging trends in ML hardware. (8 Hours)

Course Outcomes:

At the end of the course, the student will be able to:

CO1: Explain the computational requirements of machine learning algorithms and architecture.

CO2: Analyze neural network architectures and their hardware implementation challenges.

CO3: Evaluate different hardware accelerators such as GPUs, TPUs and FPGA-based ML systems.
CO4: Analyze memory hierarchy and dataflow architectures used in machine learning hardware.
CO5: Apply energy-efficient techniques and hardware optimizations for machine learning applications.
CO5: Analyze energy-efficient CMOS architecture for biomedical sensing systems

Suggested Learning Resources:

Textbooks

1. Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel Emer, Efficient Processing of Deep Neural Networks, Morgan & Claypool Publishers.
2. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann.

Reference Books

1. David B. Kirk and Wen-mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, Morgan Kaufmann.
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, Deep Learning, MIT Press.

Web Resources

1. **NPTEL – Deep Learning Hardware**
   https://nptel.ac.in
2. **NVIDIA Deep Learning Developer Resources**
   https://developer.nvidia.com/deep-learning
3. **Google TPU Architecture Overview**
   https://cloud.google.com/tpu/docs

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - II

Analog IC Design Lab (0:0:1) 1
(Effective from the academic year 2025-26)

Course Code	**MVSDL207**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:0:2	SEE Marks	50
Total Number of Lecture Hours	20	Exam Hours	03

Course objectives:

This course will enable students to

1. Understand and implement the CMOS analog circuit design flow including schematic design, simulation, layout creation, and post-layout verification using VLSI CAD tools.
2. Design and analyze basic analog circuits such as single-transistor amplifiers (Common Source, Common Drain, and Common Gate) using DC, AC, and transient analysis.
3. Design and evaluate differential amplifiers and operational amplifiers and analyze important parameters such as bandwidth.
4. Perform layout design, RC extraction, and physical verification for CMOS circuits using appropriate technology.
5. Compare pre-layout and post-layout simulation results and understand the impact of parasitic effects on circuit performance

List of Experiments:

1. Design and simulate an RC circuit and extract the propagation delay caused by resistance and capacitance.
2. Design and analyze a MOSFET current mirror circuit and verify that the output current mirrors the reference current.
3. Design the Common Source Amplifier circuit for the given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis,
   AC Analysis, transient analysis and DRC/LVS Verification.
4. Design the Common Drain Amplifier the for given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis and DRC/LVS Verification.
5. Design the differential Amplifier the for given specifications and complete the design flow: i) Draw the schematic and verify the following: DC Analysis, AC Analysis, and DRC/LVS Verification.

6. Design a single-stage op-amp for given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis.
   a)Transient Analysis and DRC/LVS Verification. b) calculation of Bandwidth
7. Design a two-stage op-amp with given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis and DRC/LVS Verification. b) calculate Bandwidth

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - II

VLSI testing and Verification Lab (0:0:1) 1
(Effective from the academic year 2025-26)

Course Code	**MVSD208**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:0:2	SEE Marks	50
Total Number of Lecture Hours	30	Exam Hours	03

Course objectives:

This course will enable students to

1. Understand the fundamentals of VLSI testing and fault models used for detecting faults in digital circuits.
2. Implement test pattern generation algorithms such as Path Sensitization, D-Algorithm, and PODEM/FAN for combinational circuits.
3. Develop programs for fault simulation and logic simulation of simple digital circuits using basic logic gates.
4. Understand and implement Design for Testability (DFT) concepts, including scan chain insertion and scan-based testing.
5. Learn test data compression and signature analysis techniques for efficient testing of digital systems.

List of Experiments:

Students shall perform the following experiments using suitable tools

1. Fault Simulation: Perform fault simulation for a given sequential circuit by injecting stuck-at faults and identifying detectable and undetectable faults.
2. Scan Chain Based Testing: Model a simple sequential circuit and demonstrate scan chain insertion. Perform scan mode testing by shifting test patterns through the scan chain and observing outputs.
3. Signature Analysis for Test Response Compression: Implement a simple signature analysis technique to compress output bit streams and analyse its effectiveness in detecting faults.
4. Path Sensitization Algorithm: Develop an algorithm to perform path sensitization for a given combinational circuit and identify input conditions required to propagate faults to the primary outputs.
5. Implementation of D-Algorithm for ATPG: Implement the D-Algorithm to generate test patterns for a given combinational circuit under stuck-at-0 and stuck-at-1 fault models.

Verification Experiments:

For the following experiments.

1. Combinational and Sequential logic design (2 experiments each)
2. Simple communication protocol (UART / SPI etc.– Basic).

Perform the following tasks:

1. Implement System Verilog Interface.
2. Generate constrained random stimulus for testing the design.
3. Implement functional coverage to measure verification completeness.
4. Use System Verilog Assertions (SVA) to verify design properties.
5. Implement Mailbox and Interposes Communication for data transfer between components.
6. Develop the Driver and Monitor for stimulus application and output observation.
7. Implement a Scoreboard to compare expected and actual results for verification.